

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1-12 (Cancelled)

1                   13. (New) A computer-implemented method for physical synthesis of  
2 integrated circuits, the method comprising:  
3                   receiving information indicative of an integrated circuit;  
4                   tracing signal flow in the integrated circuit to determine a set of critical signal  
5 paths;  
6                   placing and routing one or more circuit cells in a physical layout associated with  
7 the integrated circuit based on a priority associated with a critical signal path in the set of critical  
8 signal paths.

1                   14. (New) The method of claim 13 wherein placing and routing the one or  
2 more circuit cells in the physical layout associated with the integrated circuit based on path  
3 priorities associated with paths in the set of critical signal paths comprises placing and routing  
4 one or more elements of an RF circuit.

1                   15. (New) A computer-implemented method for physical synthesis of  
2 integrated circuits, the method comprising:  
3                   receiving information indicative of an integrated circuit;  
4                   generating a plurality of circuit layout constraints using an open circuit time  
5 constant technique on each node in a plurality of critical nodes associated with the integrated  
6 circuit;  
7                   tracing signal flow within the integrated circuit to determine a set of critical signal  
8 paths;

9                   partitioning the physical layout associated with the integrated circuit based on  
10 functionality and criticality; and

11                   placing and routing one or more circuit cells automatically in the physical layout  
12 associated with the integrated circuit based on a priority associated with a critical signal path in  
13 the set of critical signal paths.

1                 16. (New) The method of claim 15 further comprising:  
2                   calculating equivalent resistive impedance at each node of in the plurality of  
3 critical nodes in response to a DC operating point simulation.

1                 17. (New) The method of claim 15 further comprising:  
2                   calculating equivalent resistive impedance at each node in the plurality of critical  
3 nodes in response to a transient simulation.

1                 18. (New) The method of claim 15 wherein generating the plurality of circuit  
2 layout constraints using the open circuit time constant technique on each node in the plurality of  
3 critical nodes associated with the integrated circuit comprises assessing a time constant of each  
4 node in the plurality of critical nodes.

1                 19. (New) The method of claim 18 further comprising:  
2                   estimating a circuit bandwidth based on the time constant at each node in the  
3 plurality of critical nodes;  
4                   comparing the estimated circuit bandwidth with a series of design specifications  
5 associated with the integrated circuit.

1                 20. (New) The method of claim 15 wherein generating the plurality of circuit  
2 layout constraints using the open circuit time constant technique on each node in the plurality of  
3 critical nodes associated with the integrated circuit comprises determining an optimal range for  
4 parasitic loading values.

1                   21. (New) The method of claim 15 wherein placing and routing the one or  
2 more circuit cells automatically in the physical layout associated with the integrated circuit based  
3 on the priority associated with the critical signal path in the set of critical signal paths comprises  
4 placing and routing the one or more cells in response to one or more what-if scenarios associated  
5 with placement options.

1                   22. (New) The method of claim 15 wherein generating the plurality of layout  
2 constraints using the open circuit time constant technique on each node in the plurality of critical  
3 nodes associated with the integrated circuit comprises calculating a tolerable excessive parasitic  
4 loading at each node in the plurality of nodes for circuit physical synthesis at an initial topology  
5 exploration stage.

1                   23. (New) A computer readable medium configured to store a software  
2 program executable by a processor of a computer system to become operational with the  
3 processor for physical synthesis of integrated circuits, the computer readable medium  
4 comprising:

5                   program code for receiving information indicative of an integrated circuit;  
6                   program code for generating a plurality of circuit layout constraints using an open  
7 circuit time constant technique on each node in a plurality of critical nodes associated with the  
8 integrated circuit;

9                   program code for tracing signal flow within the integrated circuit to determine a  
10 set of critical signal paths;

11                  program code for partitioning the physical layout associated with the integrated  
12 circuit based on functionality and criticality; and

13                  program code for placing and routing one or more circuit cells automatically in  
14 the physical layout associated with the integrated circuit based on a priority associated with a  
15 critical signal path in the set of critical signal paths.